Ultrafast Low-Loss 40-70 GHz Differential SPDT Switch in 0.35 μm SiGe Technology

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Abstract—This paper presents an ultrafast wideband low-loss single-pole double-throw (SPDT) differential switch in 0.35-μm SiGe bipolar technology. The proposed topology adopting current-steering technique results in total measured switching time of only 65 ps, which suggests a maximum switching rate of up to 15 Gbps, the fastest ever reported at V-band. In addition, the switch exhibits insertion loss of lower than 1.25 dB from 42 to 70 GHz and isolation of better than 20 dB from 40 to 65 GHz.

Index Terms—Absorptive, balanced circuits, current steering, heterojunction bipolar transistor (HBT), insertion loss, mm-wave integrated circuit (IC), rise time, Silicon Germanium (SiGe), single-pole double-throw (SPDT), switches, switching speed, transistor circuits, V-band, 60 GHz.

I. INTRODUCTION

A simple direct-conversion transmitter architecture for use in 60 GHz radio, Fig. 1, was recently proposed in [1]. The transmitter is capable of handling BFSK/QPSK/OQPSK, and thanks to the generous bandwidth of at least 5 GHz allocated in the 60 GHz band worldwide, [2], it is possible to realize a high-speed radio with several Gbps data rate using the architecture in Fig. 1.

The single-pole double-throw (SPDT) switch in Fig. 1 is one of the key components that predominantly determine the modulators highest data rate. The rise time and fall time of the GaAs switch in [1] are, respectively, 1.4 ns and 1.8 ns compared to 3.1 ns and 2.7 ns of the 90 nm CMOS switch reported in [3]. Over the past decade, SiGe technology has been rapidly improving with the transit frequency (fT) and maximum oscillation frequency (fMAX) of the advanced SiGe bipolar transistors now exceeded 200 GHz. When compared to III-V semiconductor processes, SiGe technology holds the promise for high level of integration, reduced cost, and power dissipation. Comparisons between SiGe and CMOS devices in [4] suggest that (1) fT/fMAX of SiGe is superior by 2-3 generations to CMOS, i.e., 0.18 μm SiGe with fT of 200 GHz is comparable to 65 nm CMOS, leading to lower mask/wafer cost (2) SiGe offers better dynamic range and higher voltage handling capability than CMOS, i.e., 0.18 μm SiGe supports for 5 V collector voltage compared to 1 V in 65 nm CMOS.

Sub-nanosecond SiGe switches for use in the 24 GHz ultra-wideband (UWB) automotive radar systems were described in [5]-[7]. Extending the work in [1], the design and characterization of an ultrafast V-band SPDT switch with total rise and fall time of just 65 ps are presented in this paper. Over a large bandwidth of almost 30 GHz, the switch exhibits excellent insertion loss of lower than 1.25 dB and isolation of higher than 20 dB.

II. DIFFERENTIAL SPDT ACTIVE SWITCH

The SPDT switch circuit is illustrated in Fig. 2. The current-steering technique is adopted for fast switching operation. The tail current (IBIAS) can be steered either to differential pairs Q1-Q2 or Q6-Q7. To steer the majority current of IBIAS to Q1-Q2, the potential applied at the base of Q1/Q2 should be at least 10 V_T (V_T = kT/q is the thermal voltage and V_T = 26 mV at room temperature) more positive than the potential at the base of Q6/Q7. In this case Q6-Q7 will be switched ON while Q1-Q2 will be switched OFF thus producing the output signal only at VOUT1 port. If IBIAS is steered to Q1-Q2, differential pair Q1-Q2 will be ON while Q6-Q7 will be OFF thus producing the output signal only at VOUT2 port.

In Fig. 2, the bases of Q1 and Q2, as well as Q6 and Q7 are connected. As a result, the switch input will always see a parallel combination of ON and OFF impedances. Differential pairs Q1-Q2 and Q6-Q7 are used as a dummy to maintain the output impedance at ON and OFF states. For example, when differential pair Q1-Q2 is switched ON, Q6-Q7 will be switched OFF and when Q1-Q2 is switched OFF, Q6-Q7 will be switched ON. Consequently, the impedances seen by VOUT1 port during ON and OFF states will be always the same. The same applies to VOUT2 port.

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As opposed to the reflective switch design in [1] and [3], it is clear from the explanation above that the proposed switch is absorptive at both its input and output meaning that the input reflection coefficient ($S_{11}$) and the output reflection coefficient ($S_{22}$) remain constant regardless of the states of the switch. In a system deployment this feature is essential in order to help mitigate unwanted transient-related effects such as pulse reflection and frequency pulling of a signal source and also to minimize the phase and amplitude imbalance due to inappropriate termination at the isolation port of the 90° coupler (Fig. 1).

Simple L-type networks ($L_1 - C_1$) are sufficient to match the switch input to 50 $\Omega$. On the other hand, the switching time of the RF envelope is, in principle, determined by two factors: (1) the inherent rise time of the transistor core and (2) the bandwidth of the output matching network. From the analysis in [7], the latter dominates the switching time and therefore a broadband T-type output matching network ($L_2 - L_3 - C_2$) is deployed in the circuit in Fig. 2. The inductors (implemented using microstrip lines) and capacitors in input and output matching networks in Fig. 2 are also used as dc-feed inductances and dc-blocking capacitances, respectively, so that no additional external components are needed. Their values are given in Table I in conjunction with the transistors size. The size of the transistors $Q_9 - Q_{12}$ doubles that of $Q_1 - Q_8$ in order to handle twice higher dc currents.

![Fig. 2. High-speed SPDT differential switch circuit with current steering](image1)

![Fig. 3. Simulated return loss of a 68 x 68 $\mu m^2$ pad in parallel with a shorted shunt stub and in series with a 280 $\mu m$ long and 4.9 $\mu m$ wide 50-$\Omega$ routing line. Port 1 is connected to the pad and port 2 to the 50-$\Omega$ routing line](image2)

![Fig. 4. Simulated output waveforms and control signal](image3)

![Fig. 5. Simulated return loss (port 1-2: $V_{IN}$, port 3-4: $V_{OUT1}$, port 5-6: $V_{OUT2}$)](image4)

![Fig. 6. Simulated noise figure](image5)
output ports. The broadband characteristic of this arrangement removes the need for the input and output pads de-embedding in the measurements.

A current source that generates the tail current is implemented using a current mirror with emitter resistive degeneration so as to prevent sudden exponential increase of current caused by small $V_{BE}$ fluctuations. The effectiveness of the broadband output matching strategy described above was verified through transient simulations in RF Spectre with a 60-GHz carrier signal and 5-Gbps pulse train. The simulated modulated output signal is depicted in Fig. 4. Fig. 5 shows that return loss of higher than 10 dB is obtained across 10 GHz bandwidth from 55 to 65 GHz at the input, across 23 GHz from 52 to 75 GHz at the output 1, and across 25 GHz from 48 to 73 GHz at the output 2. Simulated noise figure (NF) across 40 GHz bandwidth is lower than 9.8 dB and is illustrated in Fig. 6.

### III. Measured Results

The switch is designed and implemented using an Infineon 0.35-μm SiGe technology [8]. A high-speed (rather than ultra-high speed) NPN transistor is chosen from the transistor set available from the foundry since it has a higher $BV_{CEO}$ (1.4 V) and $BV_{CES}$ (5.8 V). The transit frequency ($f_t$) and the maximum oscillation frequency ($f_{max}$) are derived from the extrapolations of AC current gain and unilateral gain, respectively, $f_t$ of 170 GHz and $f_{max}$ of 250 GHz peak at a collector current density of 5 mA/μm^2. Maximum emitter mask length is 10 μm.

![Fig. 7. Chip microphotograph of the SPDT switch (850 x 920 μm^2)](image)

The chip microphotograph of the SPDT switch is shown in Fig. 7. It occupies 850 x 920 μm^2 die area including pads. The differential SPDT switch was characterized through on-chip measurements. G-S-G-S-G balun probes with 100 μm pitch were used to probe the balanced input and output ports. For the S-parameter measurements, the circuit was switched ON and OFF by applying 0.5 V dc at 15 mA and -0.5 V dc at -15.2 mA, respectively, through a G-S-G probe to the control port. The circuit was operated with $V_{CC} = 1.7$ V, $V_{EE} = -1.4$ V, $V_{BB1} = 0.9$ V, $V_{BB2} = 0.7$ V. $I_{BIAS}$ was set to 20 mA so as to operate the transistors at the maximum $f_T$.

The measured S-parameters obtained from on-wafer probing are illustrated in Figs. 8 and 9. The insertion loss, $S_{21_{ON}}$, is lower than 1.25 dB across a 28-GHz bandwidth from 42 GHz to 70 GHz. Isolation, $S_{12_{OFF}}$, of higher than 20 dB and reversed transmission, $S_{12_{ON/OFF}}$, of higher than 25 dB were measured at frequencies below 65 GHz. Isolation could further be improved by adopting cascode rather than common-emitter (CE) configuration but this may result in increased insertion loss and reduced voltage swing headroom. Measured return loss in Fig. 9 is not as good as the simulation result in Fig. 5 due to: (1) for calibration involving the balun probes, Cascade Microtech requires a hybrid Line-Reflect-Reflect-Match (LRRM)/Short-Open-Load-Reciprocal (SOLR) available within WinCal XE be used. However, due to limited software resources, LRRM alone available within WinCal v.3.2.2.6 was used in the calibration (2) the transmission line model used in the simulations for the input and output matching networks was verified through measurements provided by the foundry proved accurate only up to K-band (3), additionally phase and amplitude imbalances are introduced by the balun probes. Under perfect balance assumption, the anti-phase signals would see the shared connection node of $L_1$ ($Q_1$) and $L_2$ ($Q_2$). Fig. 2, as a virtual ground and therefore the routing line to the $V_{CC}$ pad has no detrimental effects on the output matching. When amplitude and phase imbalances are present, the connection node would be no longer virtual ground and therefore the rather long thin routing line is expected to introduce some mismatch at the output. Nevertheless, in conformity with the theory described in Section II, absorbive characteristics at both the input and output ports are observed from the measurement results in Fig. 9. The insertion loss is expected to improve once input and output mismatches are compensated.

Fig. 10 presents the input-output transfer characteristic. The measured input referred 1-dB compression point (P1dB) at 55 and 60 GHz is about 1 dbm. This power handling, similar to the power handling of the SiGe switch reported in [7], is lower than diode or FET switches but the specific applications for this switch require an input signal of only -5 dBm.

![Fig. 8. Measured insertion loss, isolation, and reversed transmission](image)
For time-domain envelope measurements, the input and output ports were connected to the Agilent E8257D signal generator and the Agilent 86100D Infinium DCA-X sampling oscilloscope, respectively. The control port was connected to the Agilent E8403A pulse generator. Figs. 11 and 12 show the modulated output signal. As limited by available test equipment, the narrowest pulse width that can be applied to the switch circuit is 300 ps correspond to a bit rate of 3.333 Gbps. The rise/fall time of 25 ps/50 ps can be determined from Fig. 11. The intrinsic rise/fall slope of the pulse signal, Fig. 13, is 0.15 ps/mV and this contributes 5 ps to the rise/fall time of the switch. The total rise and fall time of 65 ps suggests that the maximum switching rate is about 15 Gbps. The dynamic isolation of the switch that is the ratio between the ON and OFF amplitudes of the RF envelope can also be determined from the modulated output signals in Figs. 11 and 12 and their values are about 25 dB, slightly higher than the static isolation in Fig. 8. Performance comparison of the SPDT switch reported here with others is presented in Table II.

### Table II

<table>
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IV. CONCLUSION

Design and characterization of an ultrafast wideband low-loss SPDT differential switch in 0.35-µm SiGe technology have been presented in this paper. The switch exhibits excellent insertion loss of lower than 1.25 dB from 42 to 70 GHz.
GHz and isolation of higher than 20 dB from 40 to 65 GHz. The total measured switching time is only 65 ps. The switch was characterized at 3.33 Gbps but switching rates of as high as 15 Gbps should be possible.

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REFERENCES