I. Introduction

The Super-heterodyne architecture has long been a standard choice for wireless receivers. Basically, it converts received RF signal energy into baseband in several steps. The IF frequency is the intermediate frequency to which RF signals are first down-converted with a high frequency local oscillator (LO). After channel selection filtering, these IF signals are down converted into the baseband with an IF LO. This approach provides not only high channel selectivity and sensitivity, but also immunity to DC offset, LO leakage and I/Q mismatch. However, in heterodyne systems, the chip-external circuitry is often complicated and costly since IF filtering is required.

The off-chip components can be reduced to a minimum using a homodyne concept. The homodyne architecture converts the received RF signals directly to baseband without any intermediate stage. This is apparently simpler and this approach requires fewer RF components than the heterodyne architecture, therefore; it leads to lower DC consumption and the possibility of monolithic one-chip integration due to the removal of the requirement of an external filter. However these advantages are at the cost of a reduced LO to RF suppression, higher TX feed through, and a less precise quadrature phase generation at the high operating frequency of 60 GHz. In this work, in order to develop a monolithic one-chip integration solution, the homodyne architecture has been chosen.

II. System Architecture

The block diagram of the system architecture is shown on Fig. 1. A fundamental 60 GHz VCO is used for LO signal generation. A buffer amplifier isolates the oscillator core from the rest of the circuit. The LO signal is split by a passive power divider and polyphase filters are used to provide the quadrature phases for the Gilbert-based up- and down-conversion mixers. The differential TX baseband signals are amplified, up-converted, and summed up using an active in-phase signal combiner before the RF signal is amplified by a Class-AB power amplifier and finally fed to the RF output pads of the chip. The RX signal is amplified by the Low Noise Amplifier (LNA), split by a passive power divider and fed to the down-conversion mixers. Only one common supply is used for all different building blocks of the transceiver.
III. Circuit Description

1. 60 GHz signal generation

   The voltage-controlled oscillator is based on a differential Colpitts topology. In order to achieve low phase noise and sufficient tuning range over process and temperature variations, the circuit uses differential high-Q varactors. To ease the implementation of a Phase Locked Loop (PLL), separate coarse and fine tuning inputs with different tuning sensitivities are provided. With this option, the VCO can be pre-adjusted by applying an appropriate tuning voltage to the coarse-tune input (e.g. filtered DAC output) and the PLL is closed using the fine tune input with less tuning slope. This can help to avoid degradation of the inherent VCO phase noise by parasitic noise injection.

   The buffer consists of an emitter-follower pair, an emitter-coupled trans-admittance stage, and a differential common base stage, additionally biased by a constant current. Its output drives the input of a differential rat-race-type power splitter that delivers the LO signal for the following RC polyphase filters, which generate the quadrature output for the up- and down-conversion mixers.

   RC polyphase filters are chosen for I/Q signal generation. The transfer loss of the final filter is 5.2 dB at the centre frequency of 60 GHz and the maximum absolute phase variation is 0.48 from 57 to 64 GHz.
2. Gilbert-based up-conversion mixer

The two up-conversion mixers are based on a Gilbert-type topology. The differential 100 V IF input is DC coupled, the trans-conductance stage converts the input voltage to an output current. The typical small signal gain of the up-converter is 0.5 dB. A minimum LO signal drive of 0 dBm is required, which is fed to the switching transistors. It transforms the input impedance to 100 ohm. Since no intentional bandwidth limitation has been implemented on the chip, the mixer offers a -3 dB modulation bandwidth from DC to 10 GHz.

3. Power amplifier

After baseband up-conversion and signal combination, the 60 GHz carrier is amplified by a linear Class-AB cascade power amplifier. Common emitter transistors are biased by a current mirror that enables linearization, since the DC current is allowed to increase with rising signal drive. Broadband input matching is done using a shunt inductance and a following low-pass matching network.

4. Low-noise amplifier

In order to achieve sufficiently high gain for the low noise amplifier (LNA) to overcome the signal loss due to the power splitter and the noise figure of the mixer, three common-emitter stages are used. For power saving reasons the current of the third stage was reused for both the first and second stage. Furthermore, the second stage offers two gain steps. Switching the second stage has the advantage that both the input and the output remain well matched in both gain step modes and the more complex gain step circuitry has less influence on noise figure.